The listing of claims will replace all prior versions, and listings, of claims in the application:

In the Claims

1. (Original) An image reject circuit comprising:

a local oscillator for producing a local oscillator signal;

a tunable phase shifting network for receiving the local oscillator signal and producing an output in-phase (I) signal and an output quadrature (Q) signal;

a first amplitude detector for determining the amplitude of the output I signal;

a second amplitude detector for determining the amplitude of the output Q signal; and,

means for determining the difference between the amplitudes of the output I and Q signals, to produce a tuning signal for tuning the phase shifting network to bring the difference between the amplitudes of the output I and Q signals towards a desired level.

A1

2. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim 1, wherein the phase shifting network has first and second input terminals for receiving the local oscillator signal, ~~and~~ wherein the phase shifting network comprises:

a first phase shifting circuit connected between the first input terminal and a voltage reference;

a second phase shifting circuit connected between the voltage reference and the second input terminal;

first and second pairs of complementary output lines connected to each of the first and second phase shifting circuits; and;

a tuning input for receiving a tuning signal.

3. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim 2, wherein each of the first and second phase shifting circuits comprises a bridge circuit, ~~each~~ said bridge circuit further comprising:

a first parallel arm and a second parallel ~~arms~~ arm connected between the respective input terminal and the voltage reference;

the first parallel arm comprising a resistive element connected in series with a capacitive element;

the second parallel arm comprising a capacitive element connected in series with a resistive element; and;

each I and Q output line being connected to a respective junction between the series connected resistive element and capacitive element.

4. (Currently Amended) ~~An~~ The image reject circuit as claimed ~~in any one of claims 1 to 3~~ in claim 1, wherein the tunable phase shifting network is tuned by adjusting an RC time constant.

5. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim ~~4~~ 3, wherein the capacitive element comprises a reverse polarity junction diode, which is tuned in accordance with the tuning signal.

6. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim ~~4~~ 3, wherein the resistive element comprises a variable resistor, which is tuned in accordance with the tuning signal.

7. (Canceled)

8. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim ~~6 or 7~~ 3, wherein the resistive element comprises a MOSFET operated in its triode region.

9. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim 2, wherein each of the first and second phase shifting ~~circuits~~ circuit comprises a first and a second bridge circuit, each of said first and second bridge circuit comprising:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising a resistive element connected in series with an inductive element;

the second arm comprising an inductive element connected in series with a resistive element;

each I and Q output line being connected to a respective junction between the series connected resistive element and inductive element; and

wherein the phase shifting network is tuned by adjusting the RL time constant.

10. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim 2, wherein each of the first and second phase shifting ~~circuits~~ circuit comprises a first and a second bridge circuit, each of said first and second bridge circuit comprising:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising an inductive element connected in series with a capacitive element;

the second arm comprising a capacitive element connected in series with an inductive element;

each I and Q output line being connected to a respective junction between the series connected inductive element and capacitive element; and

wherein the phase shifting network is tuned by adjusting the LC time constant.

11. (Currently Amended) ~~An~~ The image reject circuit as claimed in ~~any one of claims 1 to 10~~ claim 1, wherein the first and second amplitude detectors comprise:

an input terminal for receiving the input signal;

a resistor and forward polarity diode connected between the input terminal and an output terminal; and;

a capacitor connected between the output terminal and ground.

12. (Currently Amended) ~~An~~ The image reject circuit as claimed in ~~any one of claims 1 to 10~~ claim 1, wherein the first and second amplitude detectors each comprise a two stage amplitude detector.

a1 13. (Currently Amended) ~~An~~ The image reject circuit as claimed in ~~any one of claims 1 to 10~~ claim 11, wherein the first and second amplitude detectors include a quadratic function circuit.

14. (Currently Amended) ~~An~~ The image reject circuit as claimed in ~~any one of the preceding claims~~ claim 1, wherein the desired difference between the amplitudes of the output I and Q signals is substantially zero.

15. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim 14, further comprising a limiting stage for removing any residual difference between the amplitudes of the I and Q signals.

16. (Currently Amended) ~~An~~ The image reject circuit as claimed in claim ~~14 or~~ 15, further comprising an RC poly-phase filter section for removing any residual difference between the amplitudes of the I and Q signals.

17. (Currently Amended) ~~An~~ The image reject circuit as claimed in ~~any one of~~ claim 1 ~~to 13~~, wherein the desired difference between the amplitudes of the output I and Q signals is set to a predetermined level, to compensate for an amplitude error found elsewhere in the system.

18. (Currently Amended) ~~An~~ The image reject circuit as claimed in ~~any one of the preceding claims~~ claim 1, wherein the circuitry is implemented in bipolar technology.

19. (Currently Amended) ~~An~~ The image reject ~~mixer~~ circuit as claimed in ~~any one of claims 1 to 17~~ claim 1, wherein the circuitry is implemented in CMOS, BiCMOS, SiGe or GaAs technology.

20. (Currently Amended) ~~An~~ The image reject circuit as claimed in ~~any one of the preceding claims~~ claim 1, wherein the circuit is implemented as an integrated circuit.

21. (Currently Amended) ~~An~~ The image reject circuit as claimed ~~in any preceding~~ claim 1, further comprising a second tunable phase shifting network located in an intermediate frequency

path, the tuning signal of the first phase shifting network also being used to tune the second phase shifting network.

22. (Currently Amended) A method of rejecting images in a receiver circuit comprising a local oscillator for producing a local oscillator signal, and a tunable phase shifting network for receiving the local oscillator signal and producing an output in-phase (I) signal and an output quadrature (Q) signal, the method comprising the steps of;

determining the amplitude of the output I signal;

determining the amplitude of the output Q signal;

determining the difference between the amplitudes of the output I and Q signals; to produce a tuning signal; and;

~~using the tuning signal to tune~~ tuning the phase shifting network using the tuning signal to bring the difference between the amplitudes of the output I and Q signals towards a desired level.

23. (Currently Amended) ~~A~~ The method as claimed in claim 22, wherein the tunable phase shifting network is tuned by adjusting an RC time constant of the phase shifting network.

24. (Currently Amended) ~~A~~ The method as claimed in claim 23, wherein the RC time constant is changed by changing the voltage across junction diodes, the change in voltage causing the capacitance of the junction diodes to change accordingly.

25. (Currently Amended) ~~A~~ The method as claimed in claim 23, wherein the RC time constant is changed by changing the resistance value of a variable resistor

26. (Currently Amended) ~~A~~ The method as claimed in claims 23, wherein the RC time constant is changed by changing the capacitance value and the resistance value.

27. (Currently Amended) ~~A~~ The method as claimed in claim 25 ~~or 26~~, wherein the resistance value is changed by operating a MOSFET in its triode region.

28. (Currently Amended) ~~A~~ The method as claimed in claim 22, wherein the phase shifting network is tuned by adjusting an RL time constant of the phase shifting network.

29. (Currently Amended) ~~A~~ The method as claimed in claim 22, wherein the phase shifting network is tuned by adjusting an LC time constant of the phase shifting network.

30. (Currently Amended) ~~A~~ The method as claimed in ~~any one of claims 22 to 29~~ claim 22, wherein the amplitudes of the I and Q signals are determined using amplitude detectors.

31. (Currently Amended) ~~A~~ The method as claimed ~~in any one of claims 22 to 30~~ in claim 22, ~~in which the receiver further comprises a second tunable phase shifting network located in an intermediate frequency path, the method comprising the further step of~~ further comprising the step of tuning ~~the~~ a second phase shifting network located in an intermediate frequency path within the receiver, the tuning being performed according to the tuning signal determined for the first phase shifting network.

32. (Currently Amended) ~~A~~ The method as claimed in ~~any one of claims~~ claim 22 ~~to 31~~, wherein the phase shifting network is tuned such that the desired difference between the amplitudes of the I and Q signals is substantially zero.

Q1

33. (Currently Amended) ~~A~~ The method as claimed in ~~any one of claims~~ claim 22 ~~to 32~~, wherein the phase shifting network is tuned such that the desired difference between the amplitudes of the output I and Q signals is set to a predetermined level, to compensate for an amplitude error found elsewhere in the system.

34. (Currently Amended) A tunable phase shifting network for use in an image reject circuit, the tunable phase shifting network comprising:

first and second input terminals for receiving an input signal and producing an output in-phase (I) signal and an output quadrature (Q) signal;

a first phase shifting circuit connected between the first input terminal and a voltage reference;

a second phase shifting circuit connected between the voltage reference and the second input terminal;

wherein each phase shifting circuit comprises:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising a resistive element connected in series with a capacitive element;

the second arm comprising a capacitive element connected in series with a resistive element; ~~and;~~

I and Q output lines being connected to respective junctions between the series connected resistive element and capacitive element; and;

wherein the phase shifting network further comprises a tuning input for receiving a tuning signal for adjusting an RC time constant of the phase shifting network, wherein the tuning signal comprises the difference between amplitudes of the output in-phase (I) signal and the output quadrature (Q) signal.

35. (Currently Amended) ~~A~~ The tunable phase shifting network as claimed in claim 34, wherein the capacitive element comprises a reverse polarity junction diode, which is tuned in accordance with the tuning signal.

36. (Currently Amended) ~~A~~ The tunable phase shifting network as claimed in claim 34, wherein the resistive element comprises a variable resistor, which is tuned in accordance with the tuning signal.

37. (Canceled)

38. (Currently Amended) ~~A~~ The tunable phase shifting network as claimed in claim 36 ~~or 37~~, wherein the resistive element comprises a MOSFET operated in its triode region.

39. (Currently Amended) A tunable phase shifting network for use in an image reject circuit, the tunable phase shifting network comprising:

first and second input terminals for receiving an input signal and producing an output in-phase (I) signal and an output quadrature (Q) signal;

a first phase shifting circuit connected between the first input terminal and a voltage reference;

a second phase shifting circuit connected between the voltage reference and the second input terminal;

wherein each phase shifting circuit comprises:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising a resistive element connected in series with an inductive element;

the second arm comprising an inductive element connected in series with a resistive element; ~~and;~~

I and Q output lines being connected to respective junctions between the series connected resistive element and inductive element; and;

wherein the phase shifting network further comprises a tuning input for receiving a tuning signal for adjusting an RL time constant of the phase shifting network, wherein the tuning signal comprises the difference between amplitudes of the output in-phase (I) signal and the output quadrature (Q) signal.

40. (Currently Amended) A tunable phase shifting network for use in an image reject circuit, the tunable phase shifting network comprising:

first and second input terminals for receiving an input signal and producing an output in-phase (I) signal and an output quadrature (Q) signal;

a first phase shifting circuit connected between the first input terminal and a voltage reference;

a second phase shifting circuit connected between the voltage reference and the second input terminal;

wherein each phase shifting circuit comprises:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising an inductive element connected in series with a capacitive element;

the second arm comprising a capacitive element connected in series with an inductive element; ~~and~~;

A1

I and Q output lines being connected to respective junctions between the series connected inductive element and capacitive element; and;

wherein the phase shifting network further comprises a tuning input for receiving a tuning signal for adjusting an LC time constant of the phase shifting network, wherein the tuning signal comprises the difference between amplitudes of the output in-phase (I) signal and the output quadrature (Q) signal.